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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/976,641	10/12/2001	Daniel Xu	INTO-0004-US	2057

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EXAMINER	
BAUMEISTER, BRADLEY W	
ART UNIT	**PAPER NUMBER**
2815	18

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/976,641	Xu et al.
Examiner	**Art Unit**
B. William Baumeister	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 6, 2003*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-14 and 16-30* is/are pending in the application.

4a) Of the above, claim(s) *1-10* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *11-14 and 16-30* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 11-14 and 16-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. Each of claims 11 and 21 recites the limitation "a pair of trenches...extending past said buried line and said region into said substrate..." in the last and next to last clause, respectively (underline added). As each of these claims set forth four "regions" (the buried line includes a lightly-doped region, a heavily doped region, and an upper lightly doped region, and a region of a second conductivity type is further set forth), there is insufficient antecedent basis for this limitation in the claim. As the first three mentioned regions all constitute the buried line, the Examiner provisionally interprets the new claim limitation "said region" to be intended to refer to the "region of a second conductivity type," but confirmation by appropriate correction is required.

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11, 12 and 16-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinsky '205 in view of Chang '995 and Slotboom et al. '326.

a. Ovshinsky discloses a memory storage array employing phase-change memory material and includes the following structures (see e.g., FIG. 1 and cols. 15-16): a p-type semiconductor substrate 10 (unnumbered in FIG 1); a plurality of buried n+ channels (wordlines) 12 that couple various memory cells (see e.g., FIG 3); an n epitaxial layer 14; isolation trenches 16 on either side of each of the buried lines 12; p+ diffusion layer 24; SiO2 insulation layer 20 having a plurality of apertures (or pores) 22; metal contact 32; memory material 36 having a lower portion which extends into the insulation pores 22; and upper contact 40. Restated, Ovshinsky discloses all of the limitations of the listed claims except for the presence of a lightly doped n-type region interposed between the n+ wordline 12 and the p-type substrate, and that the diode structure may be formed in a bulk substrate as opposed to a bulk/epi substrate.

b. Chang is directed towards a ROM diode array having n+ conductive lines 32 diffused into a p-type bulk substrate 20 with a p+ regions 40 diffused, in turn, into the n+

conductive lines 32 to form the memory diode. Chang further teaches that additional, more lightly doped n-diffusion regions 38 are formed under the n+ conductive lines 32 for the purpose of preventing current leakage between the n+ conductive lines 32 and the p-substrate 20 (e.g., col. 4, lines 10-). It would have been obvious to one of ordinary skill in the art at the time of the invention to have further included additional, more lightly doped n-type regions between the n+ channel and p-substrate of the Ovshinsky memory device for the purpose of reducing current leakage as taught by Chang.

c. The previously added language to the independent claims sets forth that the substrate is a bulk substrate, thus distinguishing the structure from a pn diode that is formed in/on a bulk substrate as well as an epitaxial layer formed on the bulk substrate, as taught by Ovshinsky. Chang teaches that pn diodes can alternatively be formed exclusively in bulk substrates without the inclusion of an epi layer, as opposed to in bulk regions and epi regions of a substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to have formed all of the pn diode's bulk and epi regions as taught by Ovshinsky/Chang solely in a bulk substrate without growing an epilayer, as taught by Chang for the purpose of simplifying the manufacturing process and thereby reducing the associated manufacturing costs.

d. The independent claims have presently been amended to further recite that a pair of trenches are disposed on either side of the buried line and extend past the "said buried line and said region into said substrate under said buried line." Ovshinsky and Chang both teach oxide

isolation regions (16 and LOCOS isolation 30, respectively) for isolating the diodes, but neither reference teaches that the isolation structure extends below the buried line.

i. Slotboom teaches pn junction diode memory structures comprising (see e.g., FIG 2a) within a type II substrate 1, a plurality of: a type I region 4 and type II layer 26 forming a pn junction 8 that are isolated by SiOx trench isolation structure 27, and a buried type I contact layer 3 for making contact to the lower side 4 of the pn junction. (While FIG 2a depicts the type II substrate being specifically n type, Slotboom further states that all of the conductivity types may be respectively reversed; col. 10, lines 26- .) The SiOx trench isolation structure extends below the buried line 3 and the second conductivity semicircular region of 26 that is adjacent to the pn junction 8, into the substrate. Slotboom teaches that the SiOx isolation structure may be formed either by a LOCOS method (FIG 1) or alternatively by a trench isolation method (FIG 2), and that the trench isolation embodiment possesses various advantages over LOCOS including a greater reduction in lateral size scale (e.g., col. 7, lines 28-) and elimination of an alignment step (col. 7, lines 15-). The depth of the isolation grooves 27 is more than 1 micron so that the length of the current path between adjoining cells is sufficiently great for avoiding breakdown between adjoining cells in spite of the small groove width (col. 7, lines 40-43).

ii. It would have been obvious to one of ordinary skill in the art at the time of the invention practicing a memory device according to Ovshinsky/Chang to have specifically substituted a trench isolation structure as taught by Slotboom for the LOCOS isolation structure

of Chen for the reasons cited in Slotboom and restated hereinabove. It would have further been obvious to one skilled the art to have formed this trench isolation structure so as to specifically extend below the pn junction and subjacent buried line into the substrate for the purpose of avoiding breakdown between adjoining cells in spite of the small groove width as taught by Slotboom.

e. Claim 20 further recites that the pore is lined with a sidewall spacer. The Examiner notes that under the broadest reasonable interpretation, the term "sidewall spacer" relates to the method by which the insulation layer and aperture is formed, and nothing in the claim precludes the sidewall spacer from being formed of the same material as that of the insulating layer. As such, because SiO2 is an amorphous material with no long-range grain boundaries, there is no structural distinction between calling the entire SiO2 layer an insulation layer, or alternatively labeling a portion of the SiO2 as an insulation layer and another portion as a sidewall spacer. Restated, as the portion of SiO2 adjacent the pore forms a sidewall and spaces the pore and its contents from the rest of the insulation layer 20, this adjacent portion can be labeled a sidewall spacer, so the Ovshinsky reference also teaches the language of this claim.

f. Regarding claim 23, in that Ovshinsky is directed towards a digital memory array, and such arrays' primary (if not only) intended use is for storing electronic data in a machine that manipulates digital data (i.e., a computer), it would have been obvious to one of ordinary skill in the art at the time of the invention that the Ovshinsky memory device may be used in a computer

for the purpose of using it for its intended purpose, regardless of whether Ovshinsky expressly, implicitly or inherently teaches as much.

g. Regarding claim 24, Ovshinsky further discloses (see e.g., FIG 4 and col. 19) an addressing matrix (interface) 52 and integrated circuitry connections (bus) 53 coupled to the storage array 51. Further, regardless of whether Ovshinsky expressly discusses the presences of a processor, one would inherently be present in the computer and coupled to the storage so that the storage will work for its intended purpose of storing memory that is to be processed by a processor.

5. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinsky/Chang/Slotboom as applied to claim 12 above, and further in view of Holmberg et al. '705. As explained above Ovshinsky/Chang/Slotboom teaches all of the limitations of claim 12 and also those limitations set forth in claim 14, but does not teach that the contact is formed under the dielectric layer as recited in claim 13. Rather, Ovshinsky teaches that metal contact 32 is formed in and over the dielectric pore and layer.

a. Holmberg et al. '705 is directed towards a programmable memory array having buried n+ wordline 56 formed on a p-type substrate 54 under n-type region 64 with a chalcogenide phase-change based memory structure formed thereover. The lower platinum silicide memory electrode 60 is formed under the insulation layer 66 and aligned with the insulation pore. It would have been obvious to one of ordinary skill in the art at the time of the invention to have employed the electrode-under insulation structure as taught by Holmberg in the

memory device of Ovshinsky at least for the purpose of not taking up addition space in the insulation pore, thereby enabling the pore to be formed of a smaller diameter and, in turn, enabling further miniaturization of the memory array.

b. Regarding claim 14, regardless of whether either of Ovshinsky or Holmberg expressly state that the function of the upper more lightly doped n-region (e.g., Ovshinsky's n epi region 14) is to reduce the reverse bias leakage of the n+ line, the underlying physics of carrier behavior in doped semiconductor junctions dictates that this function will necessarily result due to the presence of the lightly doped n-type layer.

Response to Arguments

6. Applicant's arguments filed 6/6/2003 have been fully considered but they are moot in light of the new grounds of rejection.

INFORMATION ON HOW TO CONTACT THE USPTO

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner, **B. William Baumeister,** at **(703) 306-9165.** The examiner can normally be reached Monday through Friday, 8:30 a.m. to 5:00 p.m. If the Examiner is not available, the Examiner's supervisor, Mr. Eddie Lee, can be reached at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

B. WILLIAM BAUMEISTER
PRIMARY EXAMINER

B. William Baumeister

Primary Examiner, Art Unit 2815

August 11, 2003